

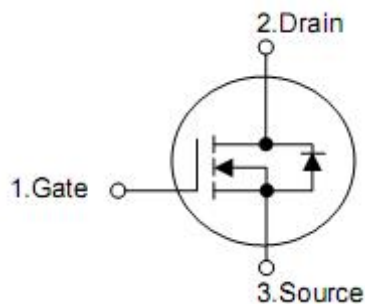
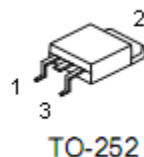
1. Description

This Power MOSFET is produced using KIA's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

2. Features

- n $R_{DS(on)}=70m\ \Omega$ @ $V_{GS}=10V$
- n High density cell design for ultra low R_{dson}
- n Fully characterized avalanche voltage and current
- n Good stability and uniformity with high E_{AS}
- n Excellent package for good heat dissipation

3. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Absolute maximum ratings

($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-source voltage	V_{DSS}	150	V
Gate-source voltage	V_{GSS}	± 20	V
Drain current continuous	I_D	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	A
Drain current pulsed	I_{DM}	40	A
Avalanche energy Single pulse (note5)	E_{AS}	200	mJ
Total power dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	W
		derate above $25\text{ }^\circ\text{C}$	$W/^\circ\text{C}$
Operating and storage temperature range	T_J, T_{STG}	-55~+175	$^\circ\text{C}$

5. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance, Junction-case (note 2)	R_{thJC}	2.0	$^\circ\text{C/W}$

6. Electrical characteristics

($T_C=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	150	165	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=150V, V_{GS}=0V$	-	-	1	μA
Gate-body leakage current	Forward	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
	Reverse	$V_{GS}=-20V, V_{DS}=0V$	-	-	-100	nA
On characteristics						
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.6	2.5	V
Static drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$	-	70	85	m Ω
Forward transconductance	g_{FS}	$V_{DS}=5V, I_D=10A$	-	20	-	S
Dynamic characteristics						
Input capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V, f=1MHz$	-	2500	-	pF
Output capacitance	C_{oss}		-	326	-	pF
Reverse transfer capacitance	C_{rss}		-	202	-	pF
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	$V_{DD}=75V, R_L=5\Omega, V_{GS}=10V, R_{GEN}=3\Omega$	-	10.5	-	ns
Rise time	t_r		-	5.5	-	ns
Turn-off delay time	$t_{d(off)}$		-	14.5	-	ns
Fall time	t_f		-	3	-	ns
Total gate charge	Q_g	$V_{DS}=75V, I_D=10A, V_{GS}=10V$	-	18	-	nC
Gate-source charge	Q_{gs}		-	4.1	-	nC
Gate-drain charge	Q_{gd}		-	4.5	-	nC
Drain-source diode characteristics and maximum ratings						
Drain-source diode forward voltage(note 3)	V_{SD}	$V_{GS}=0V, I_{SD}=20A$	-	-	1.2	V
Continuous drain-source current (note 2)	I_{SD}		-	-	20	A
Reverse recovery time	t_{rr}	$T_J=25^{\circ}\text{C}, I_F=10A, di_F/dt=100A/\mu s$ (note4)	-	32	-	ns
Reverse recovery charge	Q_{rr}		-	53	-	μC

Note: 1. repetitive rating: pulse width limited by maximum junction temperature

2. Surface mounted on FR4 board, $t \leq 10\text{sec}$.

3. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

4. Guaranteed by design, not subject to production

5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$.

7. Test circuits and waveforms

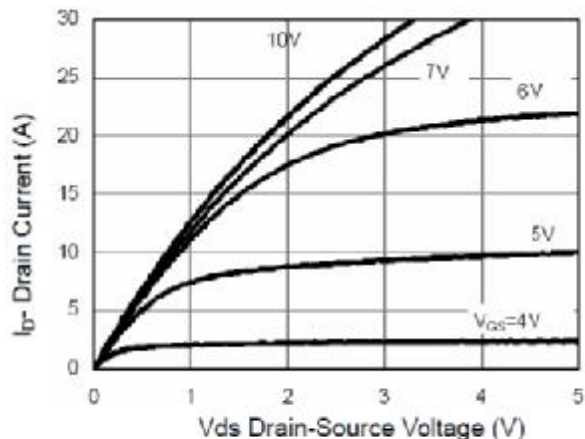


Figure 1 Output Characteristics

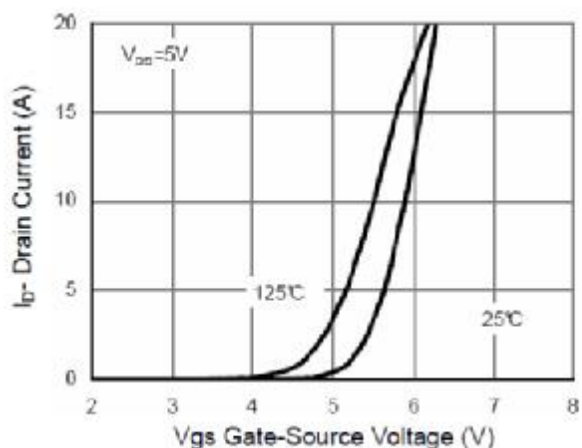


Figure 2 Transfer Characteristics

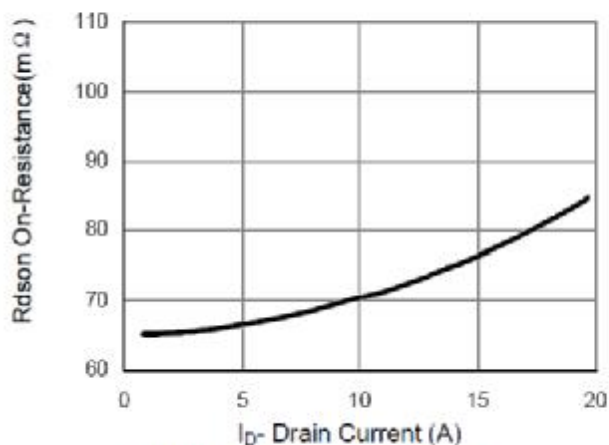


Figure 3 Rdson- Drain Current

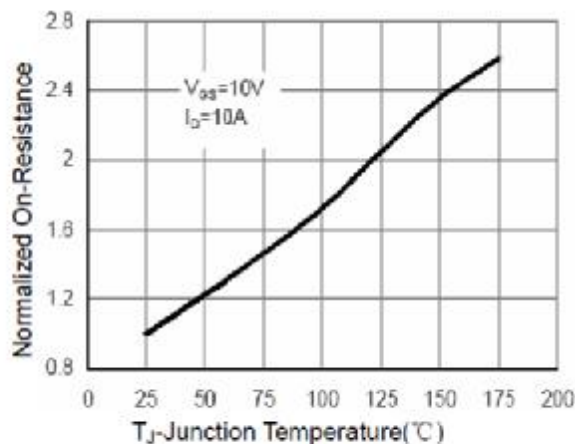


Figure 4 Rdson-Junction Temperature

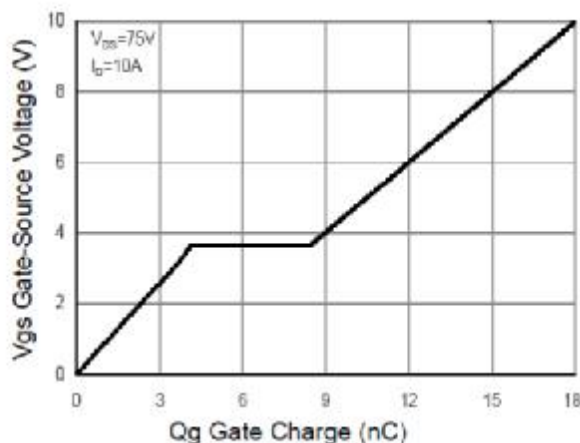


Figure 5 Gate Charge

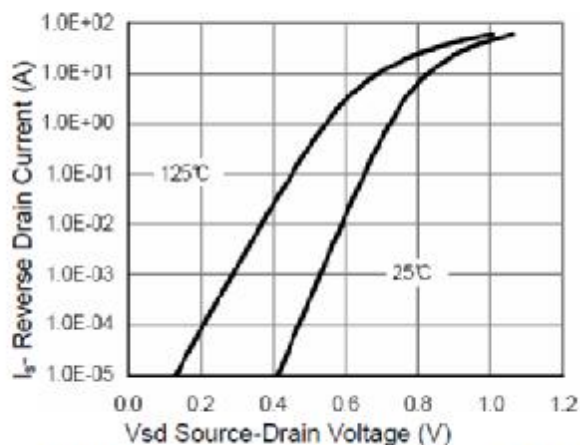


Figure 6 Source- Drain Diode Forward

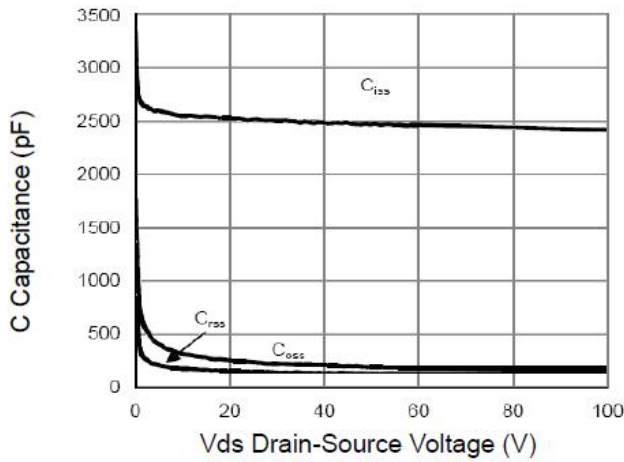


Figure 7 Capacitance vs Vds

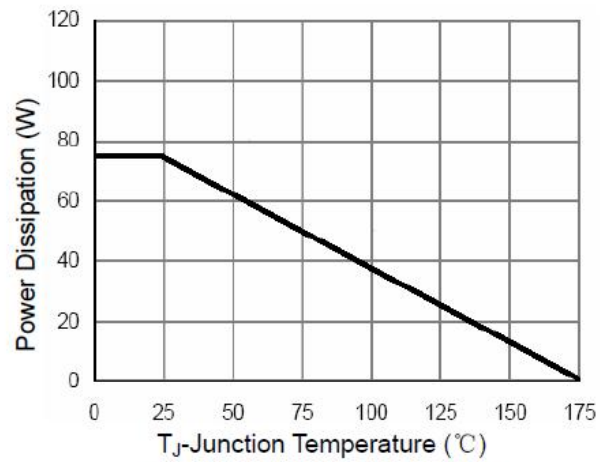


Figure 9 Power De-rating

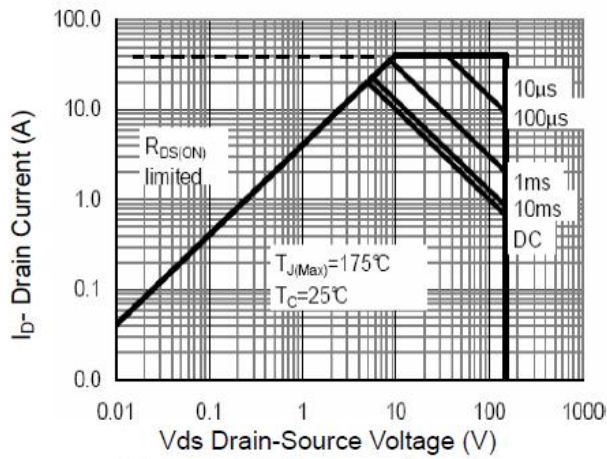


Figure 8 Safe Operation Area

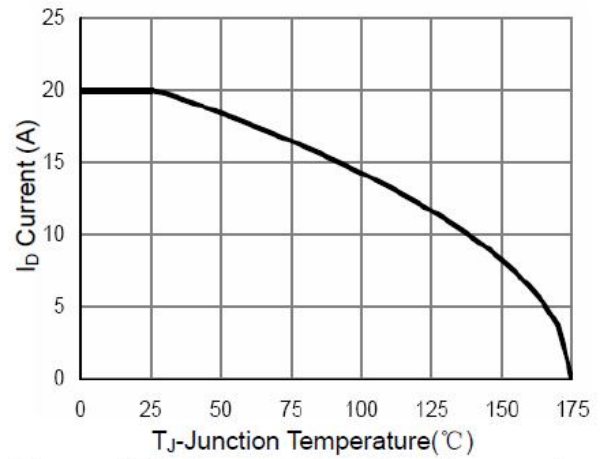


Figure 10 ID Current- Junction Temperature

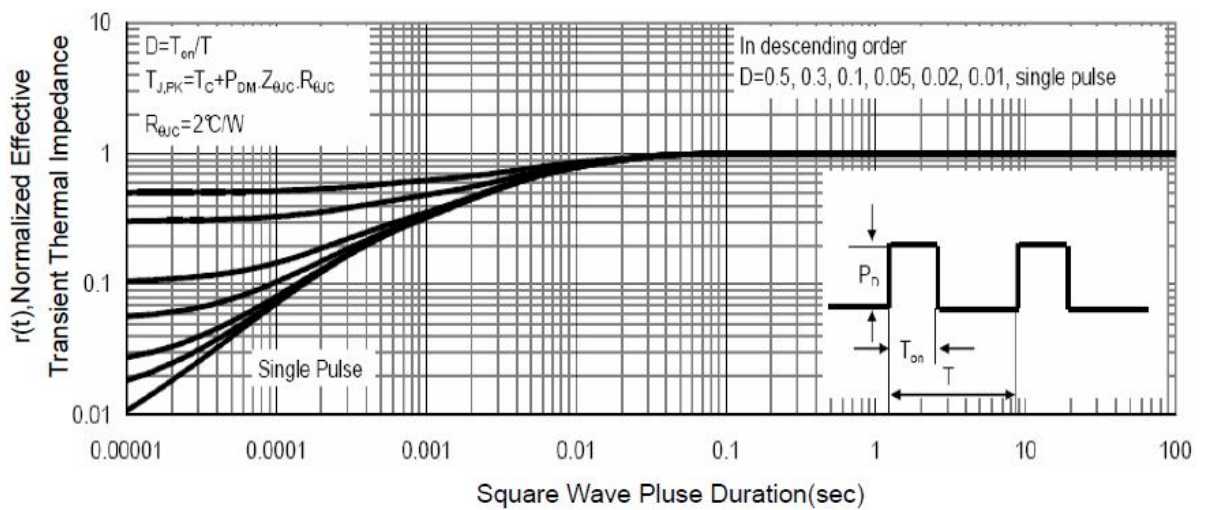


Figure 11 Normalized Maximum Transient Thermal Impedance