

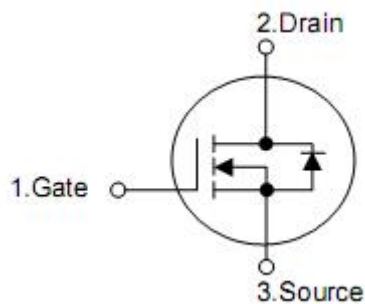
1. Description

The KND3404C is the high cell density trench N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KND3404C meet the RoHs and Green Product requirement 100% EAS Guaranteed with full function reliability approved.

2. Features

- n $R_{DS(ON),typ.}=5.0m\Omega@V_{GS}=10V$
- n Super low gate charge
- n 100% EAS Guaranteed
- n Green device available
- n Excellent Cdv/dt effect decline
- n Advanced high cell density trench technology

3. Symbol



Pin TO-252	Pin DFN5*6	Function
1	4	Gate
2	5,6,7,8	Drain
3	1,2,3	Source

4. Ordering Information

Part Number	Package	Brand
KND3404C	TO-252	KIA
KNY3404C	DFN5*6	KIA

5. Absolute maximum ratings

(T_A=25°C, unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-source voltage	V _{DS}	40	V
Gate-source voltage	V _{GS}	±20	V
Continuous drain current V _{GS} @10V ¹	T _C =25°C	I _D	80
	T _C =100°C	I _D	58
Pulsed drain current ²	I _{DM}	150	A
Single pulse avalanche energy ³	EAS	110	mJ
Avalanche current	I _{AS}	47	A
Total power dissipation ⁴	T _C =25°C	P _D	52.1
Junction and storage temperature range	T _J , T _{STG}	-55 to 150	°C

6. Thermal Data

Parameter	Symbol	Ratings	Units
Thermal resistance, junction-ambient	R _{thJA}	62	°C/W
Thermal resistance, Junction-case	R _{thJC}	2.4	°C/W

7. Electrical characteristics

(T_J=25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250uA	40	--	--	V
BVDSS Temperature Coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25°C, I _D =1mA	--	0.034	--	V/°C
Static Drain-Source On-Resistance ²	R _{DS(ON)}	TO-252 V _{GS} =10V, I _D =15A DFN5*6 V _{GS} =10V, I _D =10A	--	5.0	6.5	mΩ
		TO-252 V _{GS} =4.5V, I _D =12A DFN5*6 V _{GS} =4.5V, I _D =5A	--	6.5	9	mΩ
Gate Threshold Voltage	V _{GS(th)}	V _{GS} =V _{DS} , I _D =250uA	1.0	--	2.5	V
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)}	V _{GS} =V _{DS} , I _D =250uA	--	-5.84	--	mV/°C
Drain-Source Leakage Current	I _{DSS}	V _{DS} =32V, V _{GS} =0V, T _J =25°C	--	---	1	uA
		V _{DS} =32V, V _{GS} =0V, T _J =55°C	--	---	5	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	--	---	±100	nA
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =15A	--	25	---	S
Gate Resistance	R _g	V _{DS} =0V, V _{GS} =0V, f=1MHz	--	1.5	---	Ω
Total Gate Charge (4.5V)	Q _g	V _{DS} =20V, V _{GS} =4.5V, I _D =12A	--	28	---	nC
Gate-Source Charge	Q _{gs}		--	7.8	---	nC
Gate-Drain Charge	Q _{gd}		--	12.5	---	nC
Turn-On Delay Time	T _{d(on)}	V _{DD} =15V, V _{GS} =10V, R _G =3.3Ω, I _D =1A	--	20	---	ns
Rise Time	T _r		--	11.5	---	ns
Turn-Off Delay Time	T _{d(off)}		--	84	---	ns
Fall Time	T _f		--	8.5	---	ns
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHz	--	3330	---	pF
Output Capacitance	C _{oss}		--	270	---	pF
Reverse Transfer Capacitance	C _{rss}		--	200	---	pF
Diode Characteristics						
Continuous Source Current ^{1,5}	I _S	V _G =V _D =0V, Force Current	--	--	80	A
Pulsed Source Current ^{2,5}	I _{SM}		--	--	150	A
Diode Forward Voltage ²	V _{SD}	V _{GS} =0V, I _S =1A, T _J =25°C	--	--	1	V

Note:1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

2. The data tested by pulsed, pulse width ≤300us, duty cycle ≤2%.

3. The EAS data shows Max.rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=47A.

4. The power dissipation is limited by 150 °C junction temperature.

5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation

8. Test circuits

Typical Characteristics

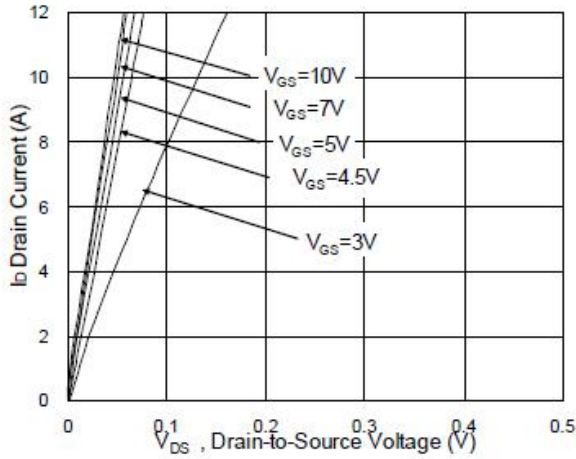


Fig.1 Typical Output Characteristics

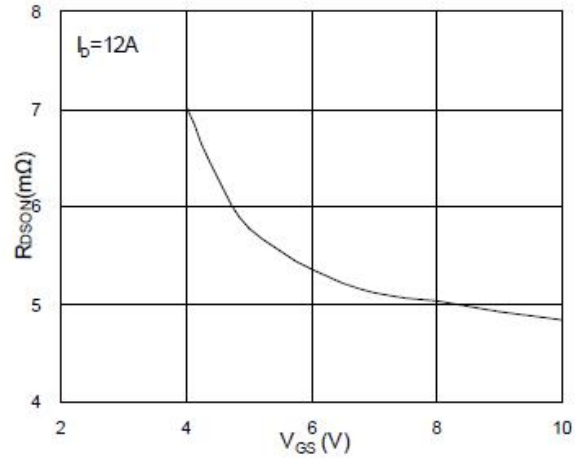


Fig.2 On-Resistance vs. G-S Voltage

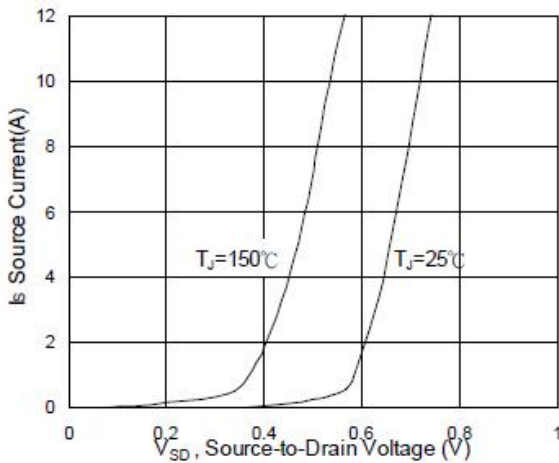


Fig.3 Forward Characteristics Of Reverse

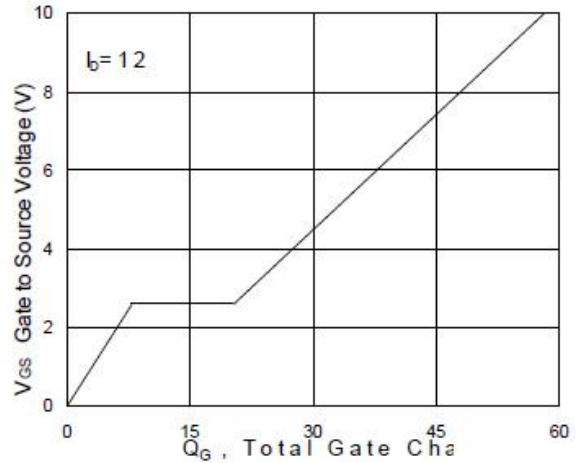


Fig.4 Gate-Charge Characteristics

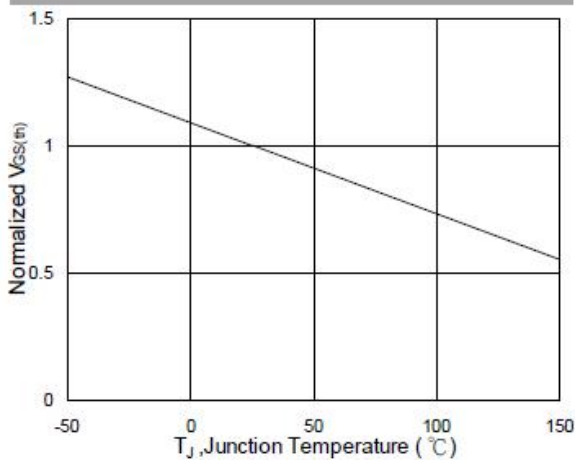


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

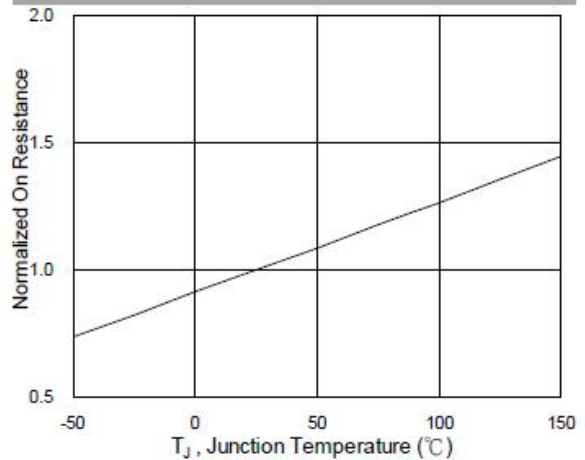


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

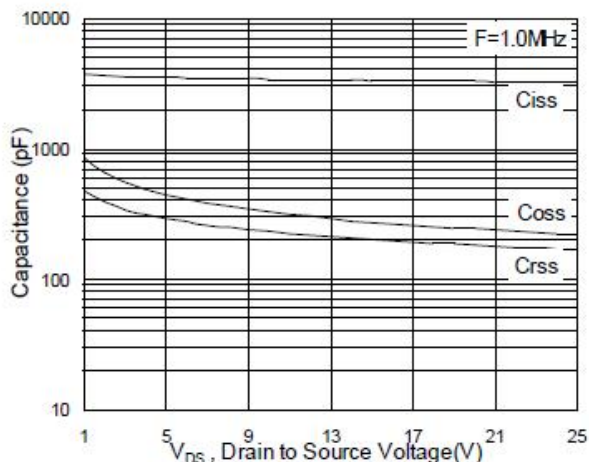


Fig.7 Capacitance

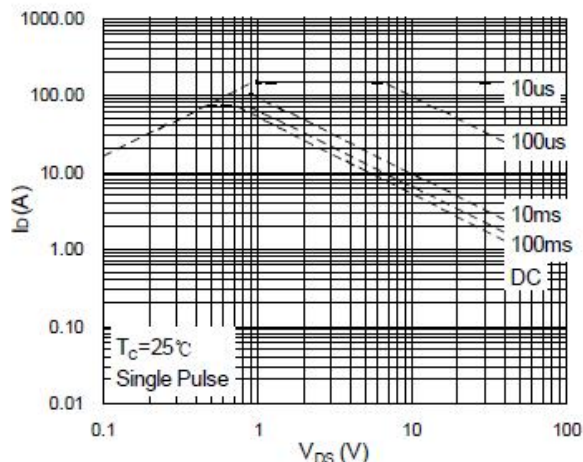


Fig.8 Safe Operating Area

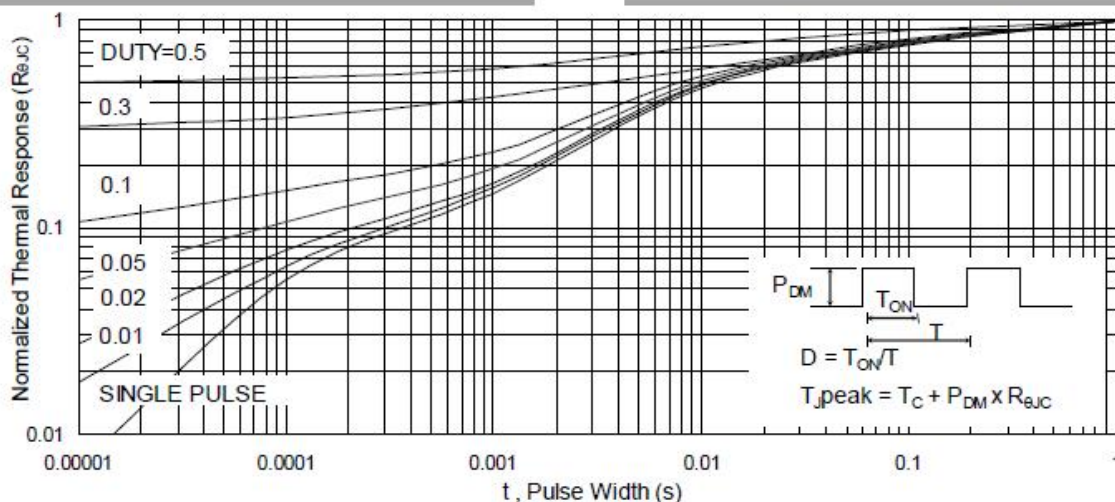


Fig.9 Normalized Maximum Transient Thermal Impedance

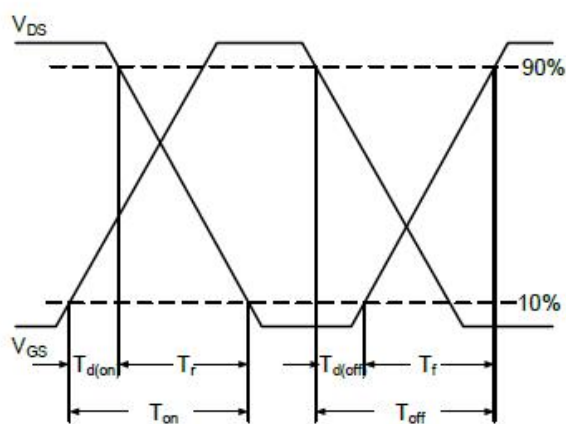


Fig.10 Switching Time Waveform

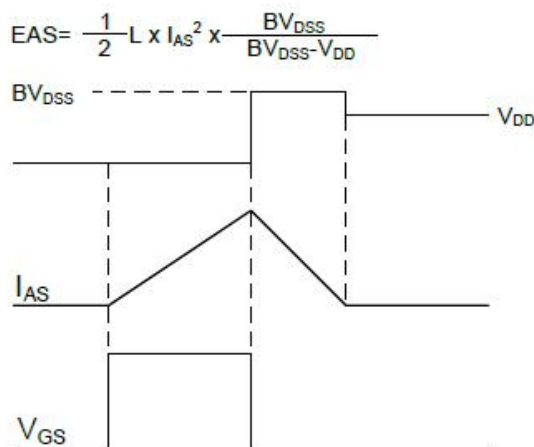


Fig.11 Unclamped Inductive Switching Wave